REMARKS

I. Introduction

Pending claims 1-9 have been examined. Claims 5-6 and 9 are allowed, while claims 2 and 4 are acknowledged to contain allowable subject matter. Claims 1, 3 and 7-8, however, are rejected. Specifically, claims 1, 3 and 7-8 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,303,234 to Kou (hereinafter "Kou") in view of U.S. Patent No. 5,347,513 to Abefelt et al. (hereinafter "Abefelt").

II. Allowable Subject Matter

Claims 5-6 and 9 are allowed.

Claims 2 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the remarks set forth below with respect to claims 1 and 3, it is respectfully submitted that claims 2 and 4 should be allowed at least by virtue of their dependency.

III. Claim Rejections – 35 U.S.C. § 103(a)

Claims 1, 3 and 7-8 stand rejected under § 103(a) as allegedly being unpatentable over Kou in view of Abefelt.

Claim 1 is directed to a slot assignment unit for use in a time division multiple access (TDMA) transmitter, comprising a unique combination of features. For example, the slot assignment unit includes a sequence controller for (i) analyzing a plurality of sets of assignment control data, (ii) producing a plurality of address pointers, (iii) storing the plurality of address

pointers in a second table in such a sequence that the address pointers can be sequentially read out in a desired transmission sequence, and (iv) supplying a command signal to a control data generation unit in response to each of the address pointers.

The Examiner alleges that the slot counter 20 of Kou corresponds to the sequence controller of claim 1 (Office Action: page 3).

As seen in Fig. 1 of Kou, the slot counter 20 receives as input a dataslot timing signal DS from slot timing circuit 19 and provides an output to buffer 16 (Kou: col. 4, lines 38-46; and Fig. 1). In Kou, a decision circuit 10 determines whether or not a packet has been properly received and generates a positive or negative acknowledgement (*i.e.*, ACK or NAK) to that effect (Kou: col. 3, lines 22-24; and col. 4, lines 12-37). This ACK/NAK data can be used, for example, to determine whether retransmission of a packet is necessary (Kou: col. 5, lines 31-46).

The ACK/NAK data from the decision circuit 10 is stored into a buffer 16 in a location determined by an address pointer from the timeslot counter 20 using a dataslot timing signal DS from the timing circuit 19 (Kou: col. 4, lines 38-46). The ACK/NAK data for a given frame can then be output from the buffer 16 in response to a timing signal supplied from a frame timing circuit 17, and multiplexed into an ACK/NAK subfield of the frame and transmitted with the user data stored in a transmit buffer 13 (*Id.*).

Furthermore, in Kou, a slot assignment circuit 21 assigns as many timeslots as there are minislots detected by the decision circuit 10 (Kou: col. 4, lines 47-55). The data generated by the slot assignment circuit 21 is stored into a buffer 23 in a location determined by an address pointer supplied from the slot counter 20 (Kou: col. 4, line 67 to col. 5, line 5).

It is respectfully submitted that the slot counter 20 of Kou does not correspond to the sequence controller of claim 1.

In claim 1, the sequence controller analyzes a plurality of sets of assignment control data. According to claim 1, this assignment control data is produced according to assignment terms (for a plurality of time slots) and slot data received from an external source. The slot counter 20 of Kou, however, does not analyze a plurality of sets of assignment control data.

To the contrary, as noted above, the slot counter 20 of Kou provides address pointers for indicating where in buffers to store data. For example, slot counter 20 provides an address pointer (based on a dataslot timing signal DS from timing circuit 19) for indicating a location in buffer 16 at which ACK/NAK data from decision circuit 10 is stored, and provides an address pointer for indicating a location in buffer 23 at which data from slot assignment circuit 21 is stored (Kou: col. 4, lines 38-46). The slot counter 20 of Kou does not analyze any data, let alone a plurality of sets of assignment control data.

Abefelt fails to make up for this exemplary deficiency of Kou because Abefelt also fails to teach or suggest a sequence controller that analyzes a plurality of sets of assignment control data.

Furthermore, in claim 1, the sequence counter stores a plurality of address pointers in a second table in such a sequence that the address pointers can be sequentially read out in a desired transmission sequence. The slot counter 20 of Kou, however, does not store a plurality of address pointers in a table in such a sequence that the address pointers can be sequentially read out in a desired transmission sequence. To the contrary, as noted above, the slot counter 20 of Kou provides address pointers for indicating where in buffers to store data, which is not the same

as storing the pointers themselves. Indeed, in Kou, the actual data (*e.g.*, ACK/NAK data, slot assignment data, etc.) are stored in the buffers and not a plurality of pointers.

The Examiner implies that Abefelt makes up for this acknowledged deficiency of Kou (Office Action: pages 3-4). To the contrary, Abefelt if disparately related to a fast operating switch for establishing connections between a plurality of units which are distributed locally within a system and which are mutually connected by means of physical links (Abefelt: col. 1, lines 6-10).

In Abefelt, an address pointer 155 is used to reference an allocation memory 134K that stores type information for the timeslots on an incoming link 63 (Abefelt: col. 16, lines 1-10). The allocation memory 134K includes a separate bit position 150 that denotes the type of time slot concerned, *i.e.*, 0 indicates that a time slot is a control-time-slot and 1 indicates that the time slot is a data-time-slot (Abefelt: col. 16, lines 12-22). In Abefelt, the switch arm 157 of a multiplexor 153 is controlled by the type information stored in the allocation memory 134K (Abefelt: col. 16, lines 22-25). The address pointer 155 of Abefelt is used to identify the type of each time slot in an arriving frame based on the information stored in the allocation memory 134K, such that a time slot of the control-time-slot type is switched to a first memory 161/1 and a time slot of the data-time-slot type is switched to a second memory 163/1 (Abefelt: col. 16, lines 25-43).

The use of an address pointer 155 to access time slot type information stored in a table (for each of the 2560 time slots contained in a frame), as described in Abefelt, does not correspond to the sequence counter of claim 1, which stores a plurality of address pointers in a second table in such a sequence that the address pointers can be sequentially read out in a desired

transmission sequence. For example, the address pointer 155 of Abefelt is not stored as a plurality of address pointers in a table, let alone stored in such a sequence that they would be sequentially read out in a desired transmission sequence.

Further still, in Kou, the slot counter 20 produces an address pointer for application to buffer 16 in response to a dataslot timing signal (DS) from slot timing circuit 19 (*see* Kou: col. 4, lines 38-46). Since the slot counter is a counter that increments a count value in response to an input timing signal and this incremented count value is used as an address pointer, the address pointer represents a binary sequence number. Therefore, ACK/NAK data from decision circuit 10 are read out from buffer 16 in the same order as they are written into the buffer. On the other hand, the claimed sequence controller (*e.g.*, sequence controller 34) is not a counter. Hence, the address pointer generated by sequence controller 34 is arbitrary. It determines the output order of first table 33 regardless of its input order. Thus, old data may be inserted between newer data. Consequently, a high speed (reordering) operation is achieved by using pointer addressing instead of conventional memory swapping as illustrated in prior art Fig. 1 (*see* specification: page 2). In Kou, the slot counter 20 has no such reordering function.

In view of the above, it is respectfully submitted that claim 1 is patentable over the proposed combination of Kou in view of Abefelt. Claim 3 recites features similar to claim 1 and, thus, claim 3 is patentable over Kou in view of Abefelt based on a rationale analogous to that set forth above for claim 1. Consequently, claims 7 and 8 are patentable over the proposed combination of Kou in view of Abefelt at least by virtue of their dependency.

IV. Formal Matter

The Examiner objects to claim 1 because it contains a typographical error. Applicant amends claim 1 to correct this typographical error, thereby overcoming the Examiner's objection to the claim.

V. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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